IN THE CLAIMS

1. (Currently amended) A semiconductor memory device with a capacitor on a bit line (COB) cell structure, comprising:

a semiconductor substrate including an isolation region that defines an active area with a plurality of source/drain regions;

a contact pad layer formed on the semiconductor substrate, said contact pad layer including gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions, and a first interlevel dielectric layer formed to cover ~~covering~~ the gate line structures and formed to laterally surround the first and second contact pads;

a bit line contact plug layer on the contact pad layer, said bit line contact plug layer including lower storage node contact plugs connected to the first contact pads, bit line contact plugs connected to the second contact pads, a protective layer pattern that covers at least a portion of the second contact pads to prevent the second contact pads from ~~being connected to~~ contacting the lower storage node contact plugs ~~and/or upper storage node contact plugs~~, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern ~~covering the lower storage node contact plugs and the protective layer pattern~~; and

a bit line layer formed on the bit line contact plug layer, said bit line layer including ~~the~~ upper storage node contact plugs connected to the lower storage node contact plugs, bit line structures connected to the bit line contact plugs, and a third interlevel dielectric layer formed to laterally surround ~~covering~~ the upper storage node contact plugs and formed to laterally surround and cover the bit line structures.

2. (Original) The semiconductor memory device of claim 1, wherein the protective layer pattern is formed of a material having a high etching selectivity with respect to the second interlevel dielectric layer.

3. (Original) The semiconductor memory device of claim 2, wherein the second interlevel dielectric layer is formed of a silicon oxide and the protective layer pattern is formed of silicon nitride.

4. (Original) The semiconductor memory device of claim 1, further comprising a capacitor formed on the bit line layer and connected to the upper storage node contact plugs.

5. (Currently amended) A semiconductor memory device of a COB cell structure in which a plurality of source/drain regions are arranged in a substantially straight line in the length and width directions, the semiconductor memory device comprising:

a semiconductor substrate having a plurality of source/drain regions defined by an isolation region;

a contact pad layer on the semiconductor substrate, the contact pad layer including gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions, and a first interlevel dielectric layer formed to cover ~~covering~~ the gate line structures and formed to laterally surround the first and second contact pads;

a bit line contact plug layer on the bit line contact plug layer, the bit line contact plug layer including lower storage node contact plugs connected to the first contact pads, bit line contact plugs connected to the first contact pads, a protective layer pattern formed on at least a portion of the second contact pads to prevent the second contact pads from ~~being connected to~~ contacting the lower storage node contact plugs ~~and/or upper storage node contact plugs~~, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern ~~covering the lower storage node contact plugs and the protective layer pattern~~; and

a bit line layer on the bit line contact plug layer, said bit line layer including ~~the~~ upper storage node contact plugs connected to the lower storage node contact plugs and arranged in a zigzag pattern, bit line structures connected to the bit line contact plugs, and a third interlevel dielectric layer formed to laterally surround ~~covering~~ the upper storage node contact plugs and formed to laterally surround and cover the bit line structures.

6. (Original) The semiconductor memory device of claim 5, wherein the protective layer pattern is formed of a material having a high etching selectivity with respect to the second interlevel dielectric layer.

7. (Original) The semiconductor memory device of claim 6, wherein the second interlevel dielectric layer is formed of silicon oxide and the protective layer pattern is formed of silicon nitride.

8. (Original) The semiconductor memory device of claim 5, further comprising a capacitor on the bit line layer and connected to the upper storage node contact plugs.

9. (Original) The semiconductor memory device of claim 8, wherein lower electrodes of the capacitor are arranged in a zigzag pattern.

10. (Original) The semiconductor memory device of claim 9, wherein lower electrodes of the capacitor are cylinder shaped.

11. (Withdrawn) A method of fabricating a semiconductor memory device of a COB cell structure, the method comprising:

forming a contact pad layer on a semiconductor substrate including a plurality of source/drain regions defined by an isolation region, the contact pad layer including gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions, and a first interlevel dielectric layer covering the gate line structures and the first and second contact pads;

forming a protective layer pattern and a second interlevel dielectric layer on the contact pad layer, and the second interlevel dielectric layer covering the protective layer pattern;

forming first contact holes by patterning the second interlevel dielectric layer so as to expose the second contact pads;

forming bit line contact plugs to fill the first contact holes, and bit line structures connected to the bit line contact plugs;

forming a third interlevel dielectric layer covering the bit line structures on the second interlevel dielectric layer;

forming second contact holes exposing the first contact pads by patterning the second and third interlevel dielectric layers; and

forming storage node contact plugs to fill the second contact holes, wherein the protective layer pattern protects the second contact pads from being connected to the storage node contact plugs.

12. (Withdrawn) The method of claim 11, wherein the protective layer pattern is formed of a material having a high etching selectivity with respect to the second interlevel dielectric layer.

13. (Withdrawn) The method of claim 12, wherein the second interlevel dielectric layer is formed of silicon oxide and the protective layer pattern is formed of silicon nitride.

14. (Withdrawn) The method of claim 11, further comprises, forming a capacitor connected to the storage node contact plugs after forming the storage node contact plugs.

15. (Withdrawn) A method of fabricating a semiconductor memory device of a COB cell structure in which a plurality of source/drain regions are arranged in a substantially straight line in the length and width directions, the method comprising:

forming a contact pad layer on a semiconductor substrate in which an active area with a plurality of source/drain regions and an isolation region surrounding the active area are defined, the contact pad layer including gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions, and a first interlevel dielectric layer covering the gate line structures and the first and second contact pads;

forming a protective layer pattern and a second interlevel dielectric layer on the contact pad layer, and the second interlevel dielectric layer covering the protective layer pattern;

forming first contact holes by patterning the second interlevel dielectric layer so as to expose the second contact pads;

forming bit line contact plugs, which fill the first contact holes, and bit line structures connected to the bit line contact plugs;

forming a third interlevel dielectric layer covering the bit line structures on the second interlevel dielectric layer;

forming second contact holes exposing the first contact pads by patterning the second and third interlevel dielectric layers; and

forming storage node contact plugs to fill the second contact holes, wherein the protective layer pattern protects the second contact pads from being connected to storage node contact plugs.

16. (Withdrawn) The method of claim 15, wherein the protective layer pattern is formed of a material having a high etching selectivity with respect to the second interlevel dielectric layer.

17. (Withdrawn) The method of claim 16, wherein the second interlevel dielectric layer is formed of silicon oxide and the protective layer pattern is formed of silicon nitride.

18. (Withdrawn) The method of claim 15, wherein the second and third interlevel dielectric layers are patterned to form the second contact holes in a zigzag pattern during the formation of the second contact holes.

19. (Withdrawn) The method of claim 15, which after forming the storage node contact plugs, further comprising:

sequentially forming an etch stopper and a mold insulating layer on the resultant structure;

defining an area for capacitor lower electrodes by patterning the etch stopper and the mold insulating layer to expose the storage node contact plugs;

conformably forming a conductive layer for forming the capacitor lower electrodes on the mold-insulating layer;

forming a buffer insulating layer on the conductive layer;

forming the capacitor lower electrodes by etching the buffer insulating layer and the conductive layer to separate nodes of the conductive layer from the resultant structure;

removing the remaining buffer insulating layer and the mold-insulating layer;

forming a dielectric layer on the capacitor lower electrodes; and

forming capacitor upper electrodes on the dielectric layer.

20. (Withdrawn) The method of claim 19, wherein the mold insulating layer and the etch stopper are patterned in a zigzag pattern.